AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 3 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a system bus;

a shared memory (i) coupled to said system bus and (ii) configured to store data; and

a multiprocessor logic circuit comprising (i) a plurality of processors and (ii) a message circuit comprising a message pipe-line FIFO, wherein (a) said message circuit is directly connected to said system bus and configured to pass messages between said plurality of processors and (b) each of said plurality of processors is directly connected to said system bus and configured to access said shared memory and said message circuit through said system bus.

2. (ORIGINAL) The apparatus according to claim 1, wherein said message circuit comprises a dedicated messaging circuit.

3. (CANCELED)

4. (ORIGINAL) The apparatus according to claim 1, wherein said message circuit is further configured to provide bi-directional orderly command passing.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said message circuit is further configured to generate one or more control signals configured to control an operation of said plurality of processors.

6. (ORIGINAL) The apparatus according to claim 5, wherein said control signals comprise signals selected from the group consisting of (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said message circuit is further configured to add commands written to a first address with normal priority levels and add commands written to a second address with urgent priority levels.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said normal priority levels comprise adding commands to an end of a message queue and said urgent priority levels comprise adding commands near to a front of said message queue.

9. (ORIGINAL) The apparatus according to claim 1, wherein said multiprocessor logic circuit further comprises:

an address decoder configured to decode a system address and control said message circuit.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus provides a multiprocessor communication and shared memory architecture.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein:

said multiprocessor logic block further comprises an address decoder configured to generate one or more first control signals configured to control said message circuit; and

said message circuit is configured to generate one or more second control signals configured to control said processors.

12. (CURRENTLY AMENDED) An apparatus comprising:

means for storing data with a shared memory;

means for processing data with a plurality of processors, wherein each of said plurality of processors is directly connected to a system bus;

means for passing messages between said processors, wherein said message passing means is directly connected to said system bus and said message passing means comprises a message pipe-line FIFO; and

means for coupling each of said processors to said shared memory, wherein said shared memory and said message passing means are accessible by each of said plurality of processors through said system bus.

13. (CURRENTLY AMENDED) A method for multiprocessor communication with a shared memory, comprising the steps of:

(A) storing data with said shared memory;

(B) processing data with a plurality of processors; and

(C) passing messages between said processors with a message circuit, wherein (i) said message circuit comprises a message pipe-line FIFO, (ii) each of said plurality of processors and said message circuit are directly connected to a system bus, and ~~(ii)~~ (iii) each of said plurality of processors is configured to access said shared memory and said message circuit through said system bus.

14. (PREVIOUSLY PRESENTED) The method according to claim 13, wherein step (C) further comprises:

providing bi-directional orderly command passing.

15. (ORIGINAL) The method according to claim 14, wherein step (C) further comprises:

generating one or more control signals, said control signals configured to control an operation of said processors.

16. (ORIGINAL) The method according to claim 15, wherein said control signals comprise signals selected from the group consisting of: (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals.

17. (PREVIOUSLY PRESENTED) The method according to claim 13, wherein step (C) further comprises:

adding commands written to a first address with normal priority levels; and

adding commands written to a second address with urgent priority levels.

18. (PREVIOUSLY PRESENTED) The method according to claim 17, wherein:

said adding commands with normal priority levels further comprises adding commands to an end of a message queue; and

said adding commands with urgent priority levels further comprises adding commands near to a front of said message queue.

19. (ORIGINAL) The method according to claim 13, wherein step (C) further comprises:

decoding a system address.

20. (ORIGINAL) The method according to claim 19, wherein step (C) further comprises:

controlling said messages in response to said decoded system address.